REMARKS

In the Office Action the Examiner has noted that claims 1-10 are pending in the application. Claim 8 has been allowed and claim 6 has been objected to. Claims 1-5, 7, 9 and 10 have been rejected as unpatentable over the prior art. By this Amendment, new claims 11 and 12 have been added. Thus, claims 1-12 are pending in the application. The Examiner's rejections are traversed below.

THE PRIOR OFFICE ACTION AND RESPONSE

In the prior Office Action the Examiner rejected claims 1-5 and 7 as anticipated by Takaba et al. In traversing this rejection, the Applicants made the following arguments:

1. Claim 1 recites "wherein the abnormality detection device is independent of a CPU controlling the communication bus and detects the abnormality directly from the communication bus."

2. The abnormality detection device is independent of a CPU controlling the communication bus, and detects the abnormality directly from the communication bus, without CPU or software intervention.

3. According to the invention of claim 1, it is possible to detect the abnormality in the communication bus with a high reliability even under complex conditions without increasing the load on the CPU or software.

4. Takaba does not teach or suggest detecting the abnormality directly from the communication bus, without CPU or software intervention.

THE NEW PRIOR ART REJECTIONS

On pages 2-5 of the Office Action the Examiner has withdrawn the prior rejections and has rejected claims 1-5, 7, 9 and 10 as unpatentable over newly cited U.S. Patent 4,613,858 to Davidson, et al., either taken alone or in combination with the previously cited U.S. Patent 5,565,856 to Takaba et al. Applicants note that the statement in the second paragraph on page 2 of the Office Action appears to be in error. That is, while this portion of the Office Action references the previously cited Takaba et al. patent in conjunction with the rejection under 35 U.S.C. § 102(b), all comments stating the specifics of the rejection relate to the newly cited Davidson patent. Therefore, Applicants believe that the Examiner meant to reject claims 1-3 and 7 as anticipated by Davidson et al. and the Applicants respond accordingly below.

On page 2 of the Office Action the Examiner takes the position that comparator 55 in Fig. 3 of Davidson corresponds to the claimed comparator of claim 1, and further takes the position that Column 2, lines 20-43 teach the claim 1 features "wherein the abnormality detection device is independent of a CPU controlling the communication bus and detects the abnormality directly from the communication bus."

CLAIM 1

Claim 1 is directed to an abnormality detection device for detecting an abnormality in a communication bus. The device includes a timer counter and a comparator which the Examiner alleges to be taught at column 2, lines 20-43 of Davidson et al.

Applicants submit that Davidson et al. is significantly different from the present claimed invention in that it relates merely to minimizing the effects of user design errors that permit a communication processor to continue transmission after its allotted time.

Davidson et al. is directed to multi-user digital bidirectional communication buses which utilize central bus controllers for traffic direction. Fig. 1 of Davidson et al. illustrates a central bus controller 11 which is connected to a plurality of users 15a - 15n via a communications bus 13. The bus controller 11 controls the traffic of the communications bus 13. Each of the users 15a - 15n has a structure as shown in Fig. 3 of Davidson et al. As illustrated therein, a comparator 55 is provided within a communication processor 37. The comparator 55 compares the output of an AND gate 45 with the output of a transmit logic signal generator 49. Further, the output of the AND gate 45 is based on the output of the transmit logic signal generator 49 and the output of an interlock 40 which is external to the communication processor 37 (column 3, lines 16-20). Accordingly, Davidson et al. does not detect "the abnormality directly from the communication bus" as set forth in claim 1.

On page 2 of the Office Action the Examiner takes the position that the claimed timer counter of claim 1 is taught by column 2, lines 21-22 of Davidson et al. This portion of Davidson et al. states:

> Each user contains therein data that may be transmitted within an
> allotted time interval.

Thus, this passage of Davidson et al. merely describes that each user contains data that may be transmitted within an allotted time interval. There is no disclosure of a timer counter "configured to measure a time during which a logical output of said communication bus remains at a first logic level which is a high level or a low level" as set forth in claim 1.

On page 2 of the Office Action the Examiner takes the position that the claimed

comparator is taught by comparator 55 in Fig. 3 and column 2, lines 20-43 of Davidson et al. However, this portion of Davidson et al. does not teach that the comparator is "configured to compare the time measured by said timer counter with a threshold value and to output an abnormality detection signal indicating an abnormality in said communication bus when the time surpasses said threshold value, wherein the abnormality detection device is independent of a CPU controlling the communication bus and detects the abnormality directly from the communication bus" as set forth in claim 1.

For the reasons set forth above, it is submitted that claim 1 patentably distinguishes over the prior art.

CLAIMS 2 AND 3

Claims 2 and 3 depend, directly or indirectly, from claim 1 and include all the features of that claim plus additional features which are not taught or suggested by the prior art. Therefore, it is submitted that claims 2 and 3 patentably distinguish over the prior art.

CLAIM 7

On page 3 of the Office Action the Examiner takes the position that column 2, lines 21-22 of Davidson et al. teach the claimed counter timer. However, for the reasons explained above, it is submitted that Davidson et al. does not teach or suggest "a timer counter configured to measure a time during which a logical output of said communication bus remains at a first logical level which is a high level or a low level" as set forth in claim 7.

With respect to the claimed comparator of claim 7 the Examiner takes the position that these features are taught by column 2, lines 20-43 of Davidson et al. However, this portion of Davidson et al. does not teach or suggest " a comparator configured to compare the time measured by said timer counter with a threshold value and to output an abnormality detection signal indicating an abnormality in said communication bus when the time surpasses said threshold value, wherein the timer counter and the comparator are independent of the CPU and are operatively coupled to detect the abnormality directly from the communication bus" as set forth in claim 7.

It is also submitted that Davidson et al. does not teach or suggest the claimed microcomputer of claim 7.

For the above reasons, it is submitted that claim 7 patentably distinguishes over the prior art.

CLAIMS 4 AND 5

Claims 4 and 5 stand rejected under 35 U.S.C. § 103 as unpatentable over Davidson et al. in view of Takaba et al.

Claim 5 is an independent claim which recites:

at least two timer counters each configured to measure a time during which a signal transmitted through said communication bus continues to be a first logical level; a register configured to cumulatively add the time measured by at least one of said at least two timer counters, the register being initialized at predetermined intervals; and

·a comparator configured to compare the time cumulatively added by said register with a threshold value and to output an abnormality detection signal indicating an abnormality in said communication bus when the cumulative time obtained by said register surpasses said threshold value, wherein the abnormality detection device is independent of a CPU controlling the communication bus and detects the abnormality directly from the communication bus.

Davidson et al. does not teach or suggest the claimed at least two timer counters or the claimed comparator of claim 5. With respect to claim 5, the Examiner relies on Takaba et al. as teaching a second timer counter. However, the combination of Davidson et al. and Takaba et al. still fails to suggest "at least two timer counters" and "a comparator" as set forth in claim 7. Further, these features are not taught by Takaba et al. for the reasons set forth in the prior Amendment. Therefore, it is submitted that claim 5 patentably distinguishes over the prior art.

Claim 4 depends from claim 1 and includes all the features of that claim plus additional features which are not taught or suggested by the prior art. Therefore, it is submitted that claim 4 patentably distinguishes over the prior art.

CLAIMS 9 AND 10

The Examiner has not specifically addressed claims 9 and 10 in the Office Action. However, these claims depend from either claim 5 or claim 1 and include all the features of the claim from which they depend, plus additional features which distinguish over the prior art. Therefore, it is submitted that claims 9 and 10 patentably distinguish over the prior art.

NEW CLAIMS 11 AND 12

New claim 11 is directed to an abnormality detection device and is broader than claim 1. New claim 11 recites:

> a timer counter configured to measure a time during which a logical output of said communication bus remains at a first logical level; and
>
> a comparator configured to compare the time measured by said timer counter with a threshold value and to output a signal indicating an abnormality in said communication bus when the time surpasses said threshold value, wherein the abnormality detection device is independent of a CPU controlling the communication bus and detects the abnormality directly from the communication bus.

Therefore, it is submitted that claim 11 patentably distinguishes over the prior art.

New claim 12 is broader than claim 8 and recites an abnormality detection device which comprises:

> at least two timer counters each configured to measure a time during which a signal transmitted through said communication bus continues to be a first logical level;
>
> a circuit configured to cumulatively add the time measured by at least one of said at least two timer counters; and
>
> a comparator configured to compare the time cumulatively added by said circuit with a threshold value and to output an abnormality detection signal indicating an abnormality in said communication bus when the cumulative time obtained by said circuit surpasses said threshold value,
>
> wherein said circuit supplies said cumulative time to at least one of said at least two timer counters, and

said at least one of said at least two timer counters

measures the time by using said cumulative time as an initial

value.

Therefore, it is submitted that claim 12 patentably distinguishes over the prior art.

ALLOWABLE SUBJECT MATTER

On page 5 of the present Office Action, the Examiner indicates that claim 6 contains allowable subject matter and would be allowable if rewritten in independent form including all of the limitations of the base claim. Claim 6 is directly dependent upon claim 5. Since the Applicant respectfully submits that claim 5 is patentably distinguishable over the prior art, as discussed above, it is submitted that claim 6 is patentable at least due to its dependence from claim 5 and due to the patentable subject matter recognized by the Examiner.

On page 8, independent claim 8 has been indicated as allowable.

CONCLUSION

In accordance with the foregoing, it is respectfully submitted that all outstanding objections and rejections have been overcome and/or rendered moot. And further, it is respectfully submitted that all pending claims patentably distinguish over the prior art. Thus, there being no further outstanding objections or rejections, the application is submitted as being in condition for allowance which action is earnestly solicited. An early action to that effect is courteously solicited.

Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

STAAS & HALSEY LLP

Date: _11-17-06_   By: _____

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